REMARKS

Claims 1-2, 8-10, 12, 17, and 18 have been amended. Claims 4-7 have been canceled. Claim 19 has been added. Support for the claim amendments can be found throughout the specification including on page 10 lines 3-13, page 10 lines 22 – page 11 line 1, and in the original claims. Claims 1, 8, 10, 12, and 17 are independent.

The Examiner rejected claims 1-18 under 35 U.S.C. §102(b) as being anticipated by Geoffrey J. Bunza (U.S. 5,838,948).

In the outstanding Office Action of May 16, 2005, the Examiner stated that "Applicants argue that the processor chip 100 is not described as hardware for Bunza's embodiment because it is in the background of the invention." This is a mischaracterization of the Applicant's arguments. Applicant's arguments are set forth below:

> **The Examiner states that Bunza teaches "providing a first processor on a single chip; loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip" and appears to identify "first and second target microprocessors" described by Bunza at col. 2, lines 52-55 as the first and second processors. The Examiner further identifies block 100 in Bunza's FIG. 5 as "hardware of the microprocessors." However, processor chip 100 in FIG. 5 is not described as hardware for Bunza's "first and second target microprocessors" since FIG. 5 is part of a section that is "a brief discussion of conventional simulation systems [that] serve to distinguish the present invention," (col. 5, lines 41-42) and Bunza's "first and second target microprocessors" are described as being included in an "embodiment" of the invention. Nowhere does Bunza teach or suggest that the first and second target microprocessors are on a single silicon chip.**

First, the section quoted above is part of a section that is characterized as "a brief discussion of conventional simulation systems [that] serve to distinguish the present invention," (col. 5, lines 41-42) and does not occur in the "background of the invention" section, but rather in the "detailed description of the invention" section. Second, Applicant's argument was not based on where the subject matter occurred in the reference, but rather was based on explaining how the Examiner improperly interpreted the teachings of the reference to suggest that the first

and second processor are provided in hardware on a single silicon chip. The Applicant still contends that Bunza does not teach that the first and second processor are provided in hardware on a single silicon chip.

Nevertheless, the Applicant submits that claims 1-18, as amended in this reply, further distinguish over Bunza as follows.

Claims 1-3, 9, and 17-19

Bunza neither describes nor suggests at least "a plurality of software simulations of a corresponding plurality of second processors ... and setting the corresponding software simulation that is executing the one of the software application being debugged, to a first simulation mode, and setting at least one other software simulation that is executing a different one of the software applications, which is not being debugged, to a second simulation mode," as recited in amended claim 1, or "a plurality of software simulations of a corresponding plurality of second processors ... [and a first processor] configured to execute a software application being debugged with a software simulation set to a first simulation mode, and to execute at least one other of the software applications not being debugged with a software simulation set to a second simulation mode," as recited in amended claim 17. Therefore claims 1 and 17 are patentable over Bunza.

Dependent claims 2-3, and 9 depend on claim 1, and dependent claims 18 and 19 depend on claim 17, and are therefore patentable for at least the same reasons as for claims 1 and 17.

Claim 8

Bunza neither describes nor suggests at least "providing a first processor on a single silicon chip; loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip; loading, on the first processor, a software application to be executed on the hardware of the second processor; ... providing a third processor external to the single silicon chip; ... loading, on the third processor, the software simulation of the second processor; ... loading, on the third processor, the software application;

and executing the software simulation of the second processor and the software application on the third processor," as recited in amended claim 8.

For example, in the previous Office Action of October 4, 2004, incorporated by reference into the current Office Action of May 16, 2005, with respect to claim 8, the Examiner identifies Bunza's "target circuitry" described as an IC circuit or ASIC as the "third processor" and then cites col. 6, lines 1-13 of Bunza as disclosing "executing the software simulation of the second processor and the applications software on the third processor." However, this cited portion of Bunza does not teach or suggest that any software is executed on the target circuitry, much less, that the software simulation of the second processor and the applications software is executed on the target circuitry (identified as the third processor). Bunza discloses at col. 6, lines 1-13:

> **A target program 22 is compiled into object code, and the object code is downloaded into a processor memory model 24 within the hardware simulator 20. A processor functional model 26 is a software description, including the electrical and logical properties, of the target microprocessor, while a target circuitry functional model 28 provides a model of the target circuitry, such as an ASIC, or other custom or semi-custom design. The hardware simulator 20 allows the processor functional model 26 to simulate execution of the target program 22 event by event. As discussed above, the processor functional model 26 and the target circuitry functional model 28 can be specified to various levels of abstraction by a conventional HDL. (col. 6, lines 1-13)**

This fails to suggest the software simulation of the second processor and the applications software executed on the target circuitry . Therefore, claim 8 is patentable over Bunza.

Claims 10 and 11

Bunza neither describes nor suggests at least to "set the software simulation of the first processor in either a slow, highly detailed simulation mode or a fast, high-level simulation mode based on whether the first software application is being debugged, if the first software application is configured to execute with the software simulation of the first processor," as recited in amended claim 10. Therefore, claim 10 is patentable over Bunza.

Dependent claim 11 depends on claim 10, and is therefore patentable for at least the same reasons as for claim 10.

Claims 12-16

Bunza neither describes nor suggests at least "loading, on a first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on a single silicon chip, each software simulation corresponding to a one of the second processors, and each software simulation including a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor," as recited in claim 12.

For example, in the previous Office Action of October 4, 2004, with respect to claim 12, the Examiner cites col. 11, lines 47-67 of Bunza as disclosing a "high speed processor emulator" and a "slow software simulator." However, claim 12 requires that each software simulation includes "a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor." Instead, Bunza describes:

> **The system 200 uses the processor emulator 202, which is a high speed hardware device, to emulate the target microprocessor and the hardware simulator 206, which is a relatively slow software simulator, to model the target circuitry. (col. 11, lines 48-52)**

Not only does Bunza desccribe the "processor emulator 202" as "a high speed hardware device" instead of a software simulation, but also Bunza fails to teach or suggest that any hardware or software simulation or emulator includes both a slow, highly detailed simulation and a fast, high-level simulation of any processor. Therefore, claim 12 is patentable over Bunza.

Dependent claims 13-16 depend on claim 12, and are therefore patentable for at least the same reasons as for claims 12.

Enclosed is a $790 check for Request for Continued Examination fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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